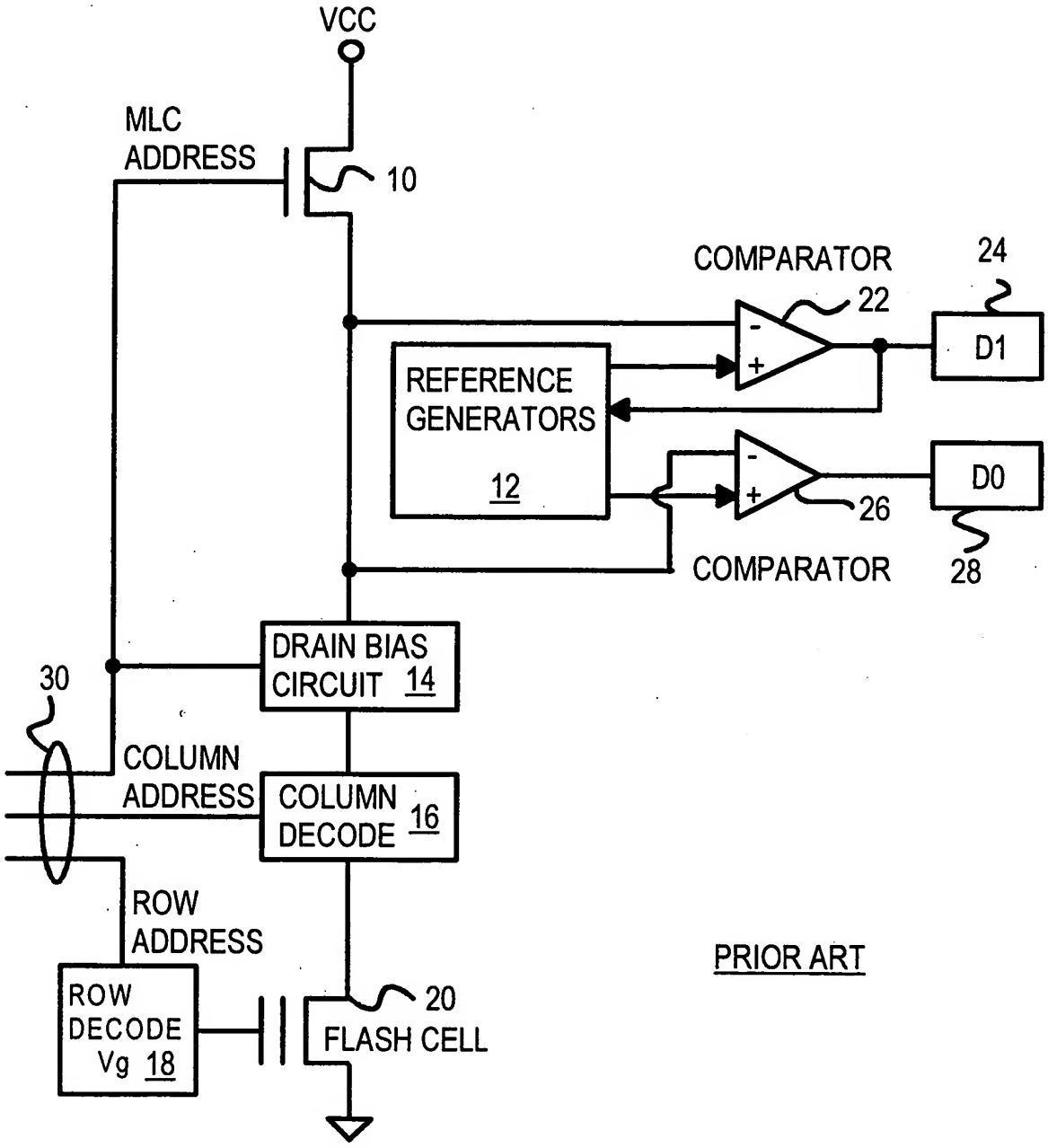
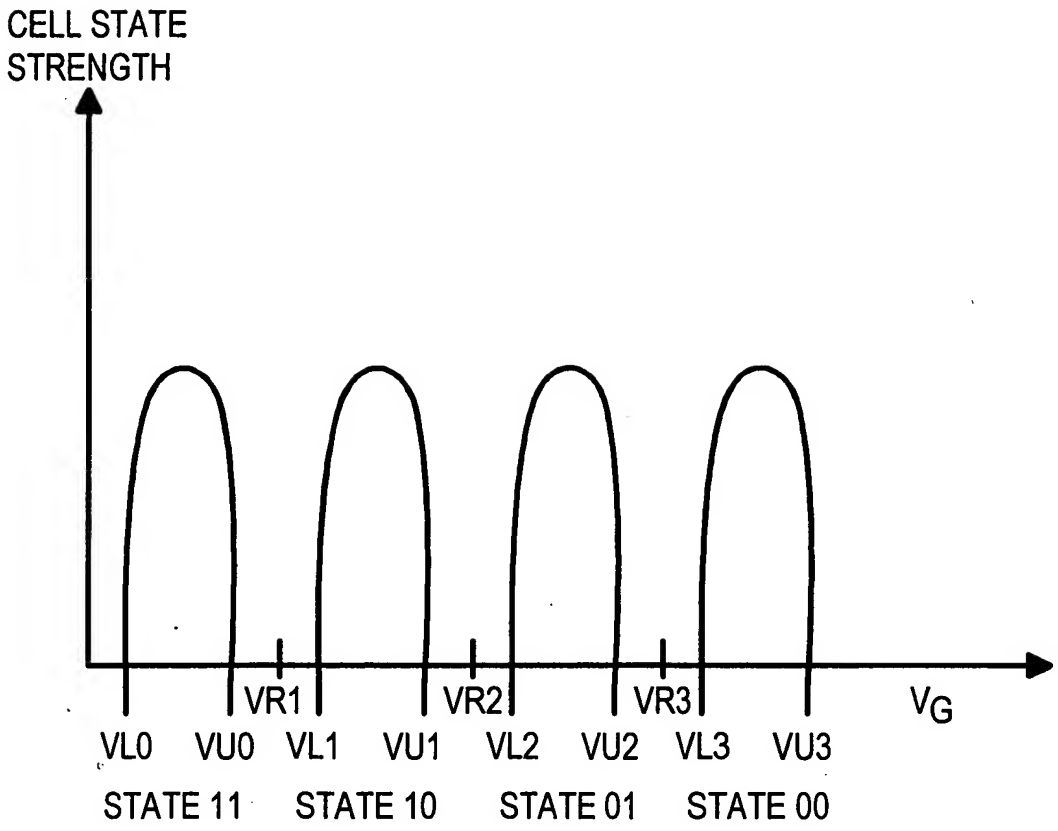
OIPE JUL 19 2004 PATENT & TRADEMARK OFFICE



PRIOR ART

FIG. 1



PRIOR ART

FIG. 2

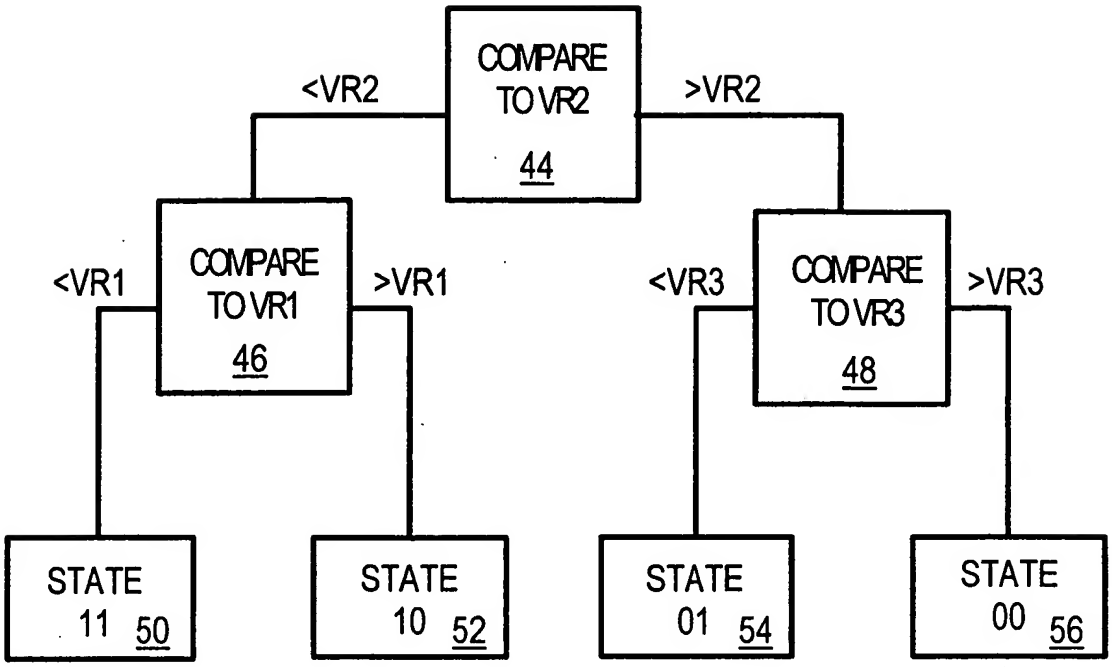


FIG. 3 PRIOR ART

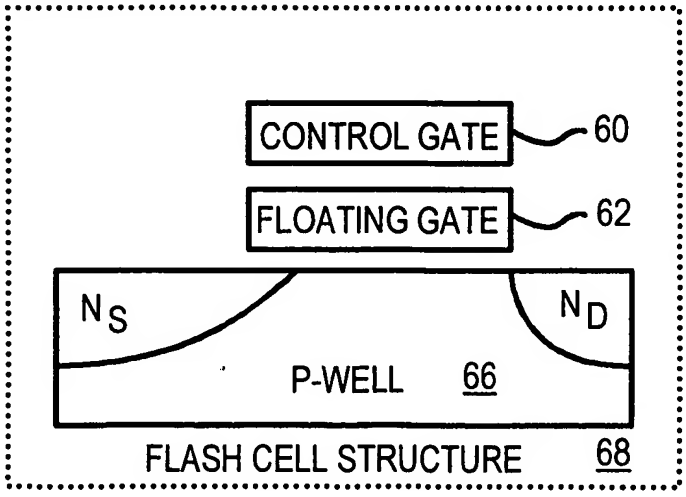


FIG. 4A

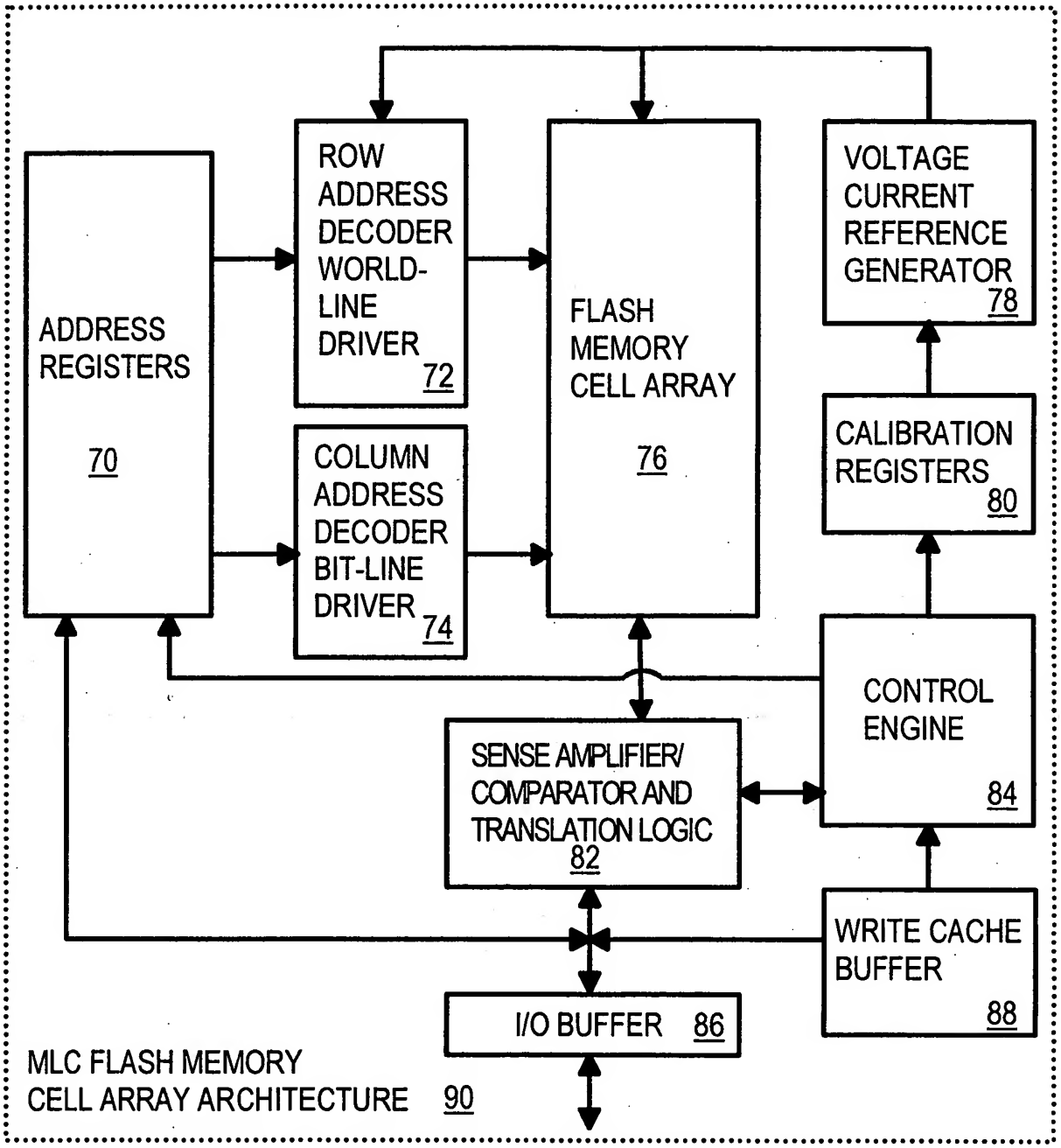

ADDRESS REGISTERS
70
ROW ADDRESS DECODER WORLD-LINE DRIVER
72
COLUMN ADDRESS DECODER BIT-LINE DRIVER
74
FLASH MEMORY CELL ARRAY
76
VOLTAGE CURRENT REFERENCE GENERATOR
78
CALIBRATION REGISTERS
80
CONTROL ENGINE
84
SENSE AMPLIFIER/ COMPARATOR AND TRANSLATION LOGIC
82
WRITE CACHE BUFFER
88
I/O BUFFER
86
MLC FLASH MEMORY CELL ARRAY ARCHITECTURE
90

FIG. 4B

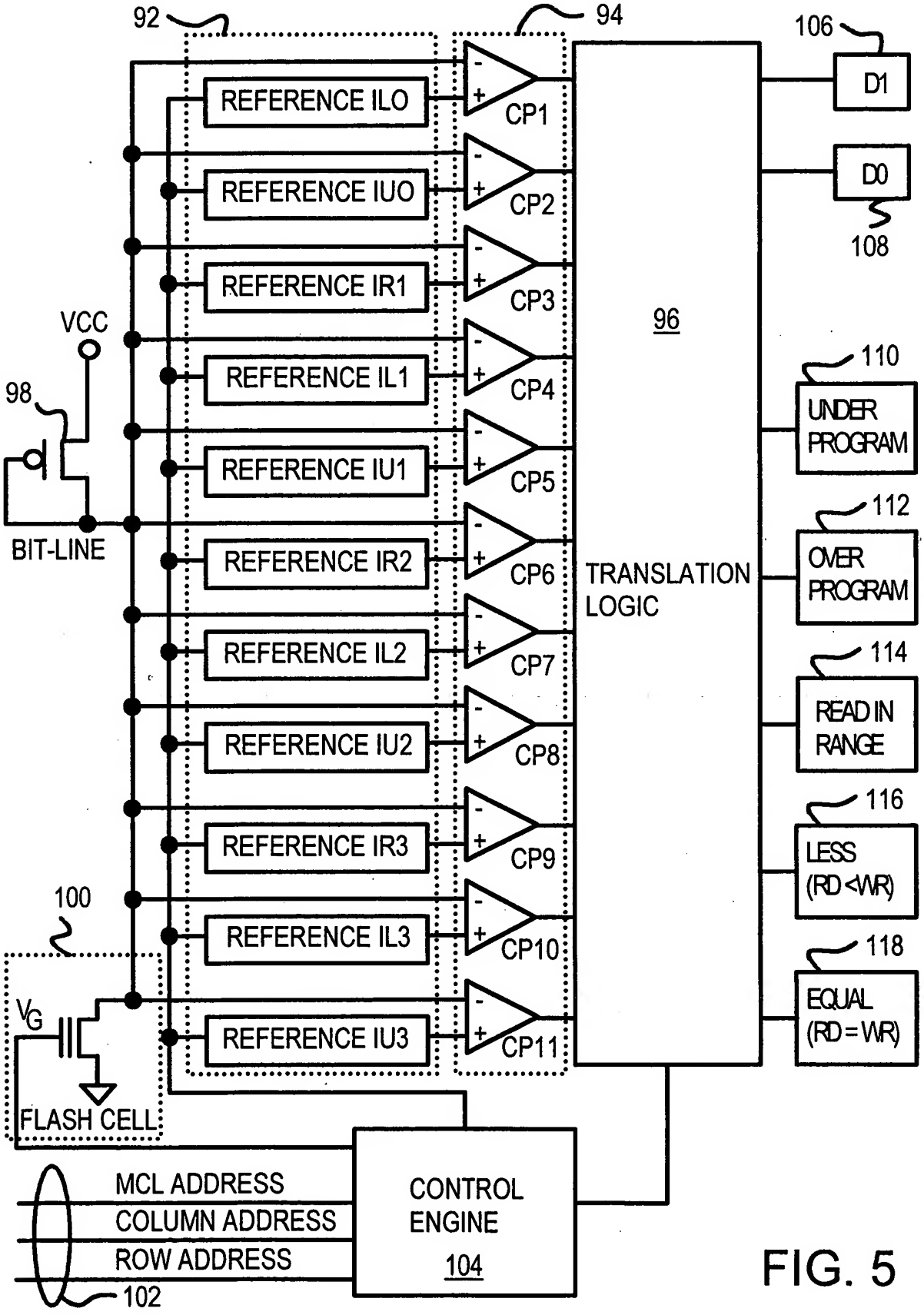

92
94
106
D1
D0
108
REFERENCE ILO
REFERENCE IUO
REFERENCE IR1
REFERENCE IL1
REFERENCE IU1
REFERENCE IR2
REFERENCE IL2
REFERENCE IU2
REFERENCE IR3
REFERENCE IL3
REFERENCE IU3
CP1
CP2
CP3
CP4
CP5
CP6
CP7
CP8
CP9
CP10
CP11
96
TRANSLATION LOGIC
VCC
98
BIT-LINE
110
UNDER PROGRAM
112
OVER PROGRAM
114
READ IN RANGE
116
LESS (RD<WR)
118
EQUAL (RD=WR)
100
V_G
FLASH CELL
MCL ADDRESS
COLUMN ADDRESS
ROW ADDRESS
102
CONTROL ENGINE
104

FIG. 5

CELL SIZE	PRIOR ART READ ACCESS TIME	INVENTION READ ACCESS TIME
2-BIT PER CELL	TC + 2TS + TR	TC + TS + TR
3-BIT PER CELL	TC + 3TS + TR	TC + TS + TR
N-BIT PER CELL	TC + nTS + TR	TC + TS + TR
DEFINITIONS	TC: READ ACCESS TIME FOR FLASH CELL TS: SENSE AMP/COMPARATOR RESPONSE TIME TR: TRANSLATION LOGIC DECODING TIME	

FIG. 6

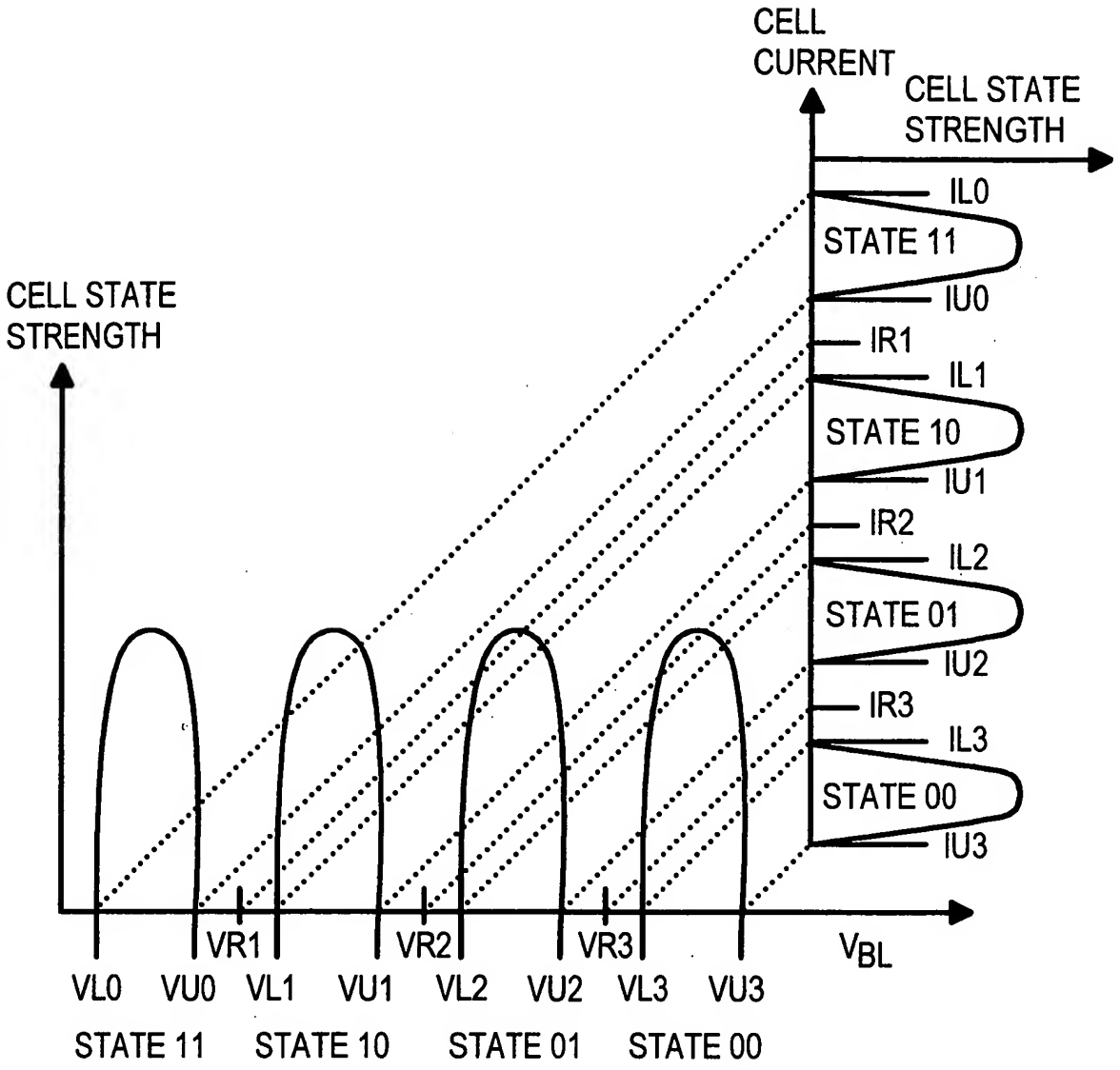

CELL CURRENT
CELL STATE STRENGTH
IL0
STATE 11
IU0
IR1
IL1
STATE 10
IU1
IR2
IL2
STATE 01
IU2
IR3
IL3
STATE 00
IU3
CELL STATE STRENGTH
VR1
VR2
VR3
V_{BL}
VL0 VU0 VL1 VU1 VL2 VU2 VL3 VU3
STATE 11 STATE 10 STATE 01 STATE 00

FIG. 7

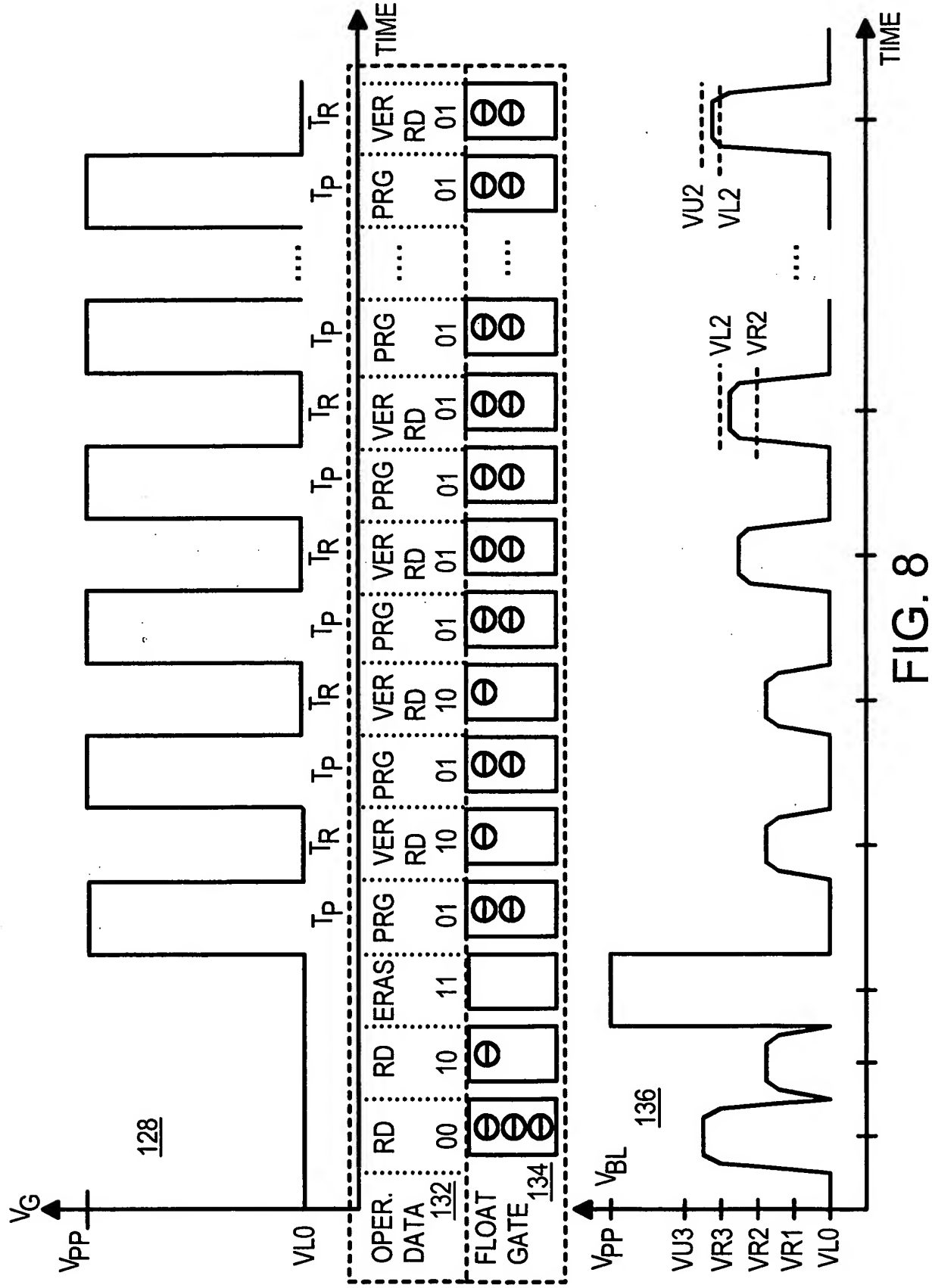

V_G
V_{PP}
128
VL0
OPER. DATA 132
FLOAT GATE 134
RD 00
RD 10
ERAS 11
PRG 01
VER RD 10
PRG 01
VER RD 01
PRG 01
T_P
T_R
TIME
V_{BL}
136
V_{PP}
VU3
VR3
VR2
VR1
VL0
VU2
VL2
VL2
VR2
TIME

FIG. 8

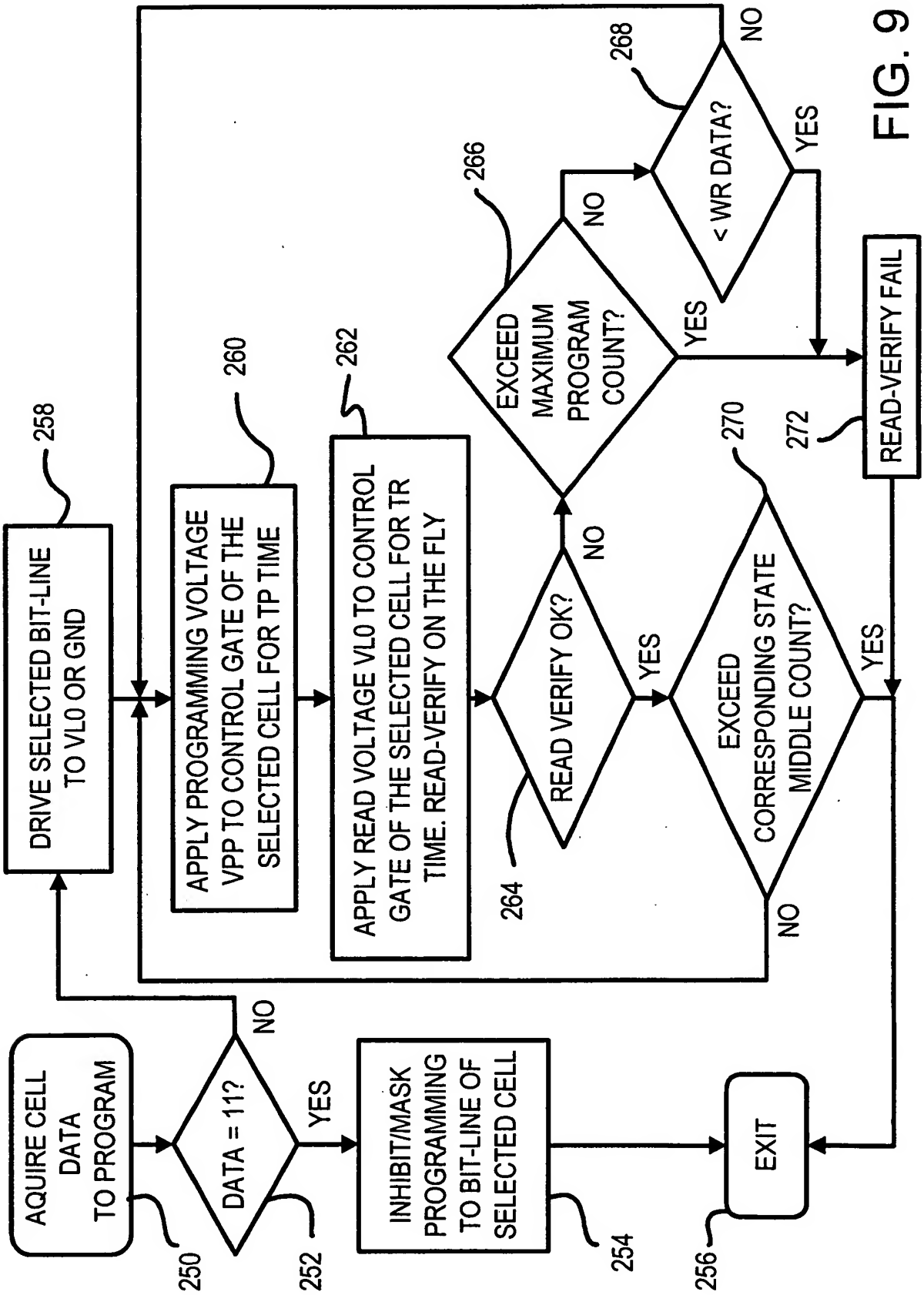

AQUIRE CELL DATA TO PROGRAM
250
DATA = 11?
252
NO
YES
INHIBIT/MASK PROGRAMMING TO BIT-LINE OF SELECTED CELL
254
EXIT
256
DRIVE SELECTED BIT-LINE TO VL0 OR GND
258
APPLY PROGRAMMING VOLTAGE VPP TO CONTROL GATE OF THE SELECTED CELL FOR TP TIME
260
APPLY READ VOLTAGE VL0 TO CONTROL GATE OF THE SELECTED CELL FOR TR TIME. READ-VERIFY ON THE FLY
262
READ VERIFY OK?
264
NO
YES
EXCEED MAXIMUM PROGRAM COUNT?
266
NO
YES
< WR DATA?
268
NO
YES
EXCEED CORRESPONDING STATE MIDDLE COUNT?
270
NO
YES
READ-VERIFY FAIL
272

FIG. 9

FIG. 10

READ SUB-STATE	IL0	IU0	IR1	IL1	IU1	IR2	IL2	IU2	IR3	IL3	IU3	RD-D1	RD-D0	READ-IN-RANGE	OVER	UNDER
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
2	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
3	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
4	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1
5	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0
6	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0
7	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	1
8	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0
9	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0
10	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1
11	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

READ-VERIFY STATE	WR-D1	WR-D0	RD-D1	RD-D0	READ-VERIFY EQUAL	READ-VERIFY LESS
1	0	0	0	0	1	0
2	0	0	0	1	0	0
3	0	0	1	0	0	0
4	0	0	1	1	0	0
5	0	1	0	0	0	1
6	0	1	0	1	1	0
7	0	1	1	0	0	0
8	0	1	1	1	0	0
9	1	0	0	0	0	1
10	1	0	0	1	0	1
11	1	0	1	0	1	0
12	1	0	1	1	0	0
13	1	1	0	0	0	1
14	1	1	0	1	0	1
15	1	1	1	0	0	1
16	1	1	1	1	1	0

FIG. 11

CURRENT REFERENCE NODE	CURRENT REFERENCE
RN-IU3	IU3
RN-IL3	IL3 = IU3 + DELTA IL3
RN-IR3	IR3 = IL3 + DELTA IR3
RN-IU2	IU2 = IR3 + DELTA IU2
RN-IL2	IL2 = IU2 + DELTA IL2
RN-IR2	IR2 = IL2 + DELTA IR2
RN-IU1	IU1 = IR2 + DELTA IU1
RN-IL1	IL1 = IU1 + DELTA IL1
RN-IR1	IR1 = IL1 + DELTA IR1
RN-IU0	IU0 = IR1 + DELTA IU0
RN-IL0	IL0 = IU0 + DELTA IL0

FIG. 12A

WEIGHT OF ID	1/2	1/4	1/8	1/16	
CALIBRATION CODE	QP31	QP32	QP33	QP34	DELTA REFERENCE CURRENT
0	0	0	0	0	0
1	0	0	0	1	1/16
2	0	0	1	0	2/16
3	0	0	1	1	3/16
4	0	1	0	0	4/16
5	0	1	0	1	5/16
6	0	1	1	0	6/16
7	0	1	1	1	7/16
8	1	0	0	0	8/16
9	1	0	0	1	9/16
10	1	0	1	0	10/16
11	1	0	1	1	11/16
12	1	1	0	0	12/16
13	1	1	0	1	13/16
14	1	1	1	0	14/16
15	1	1	1	1	15/16

FIG. 12B

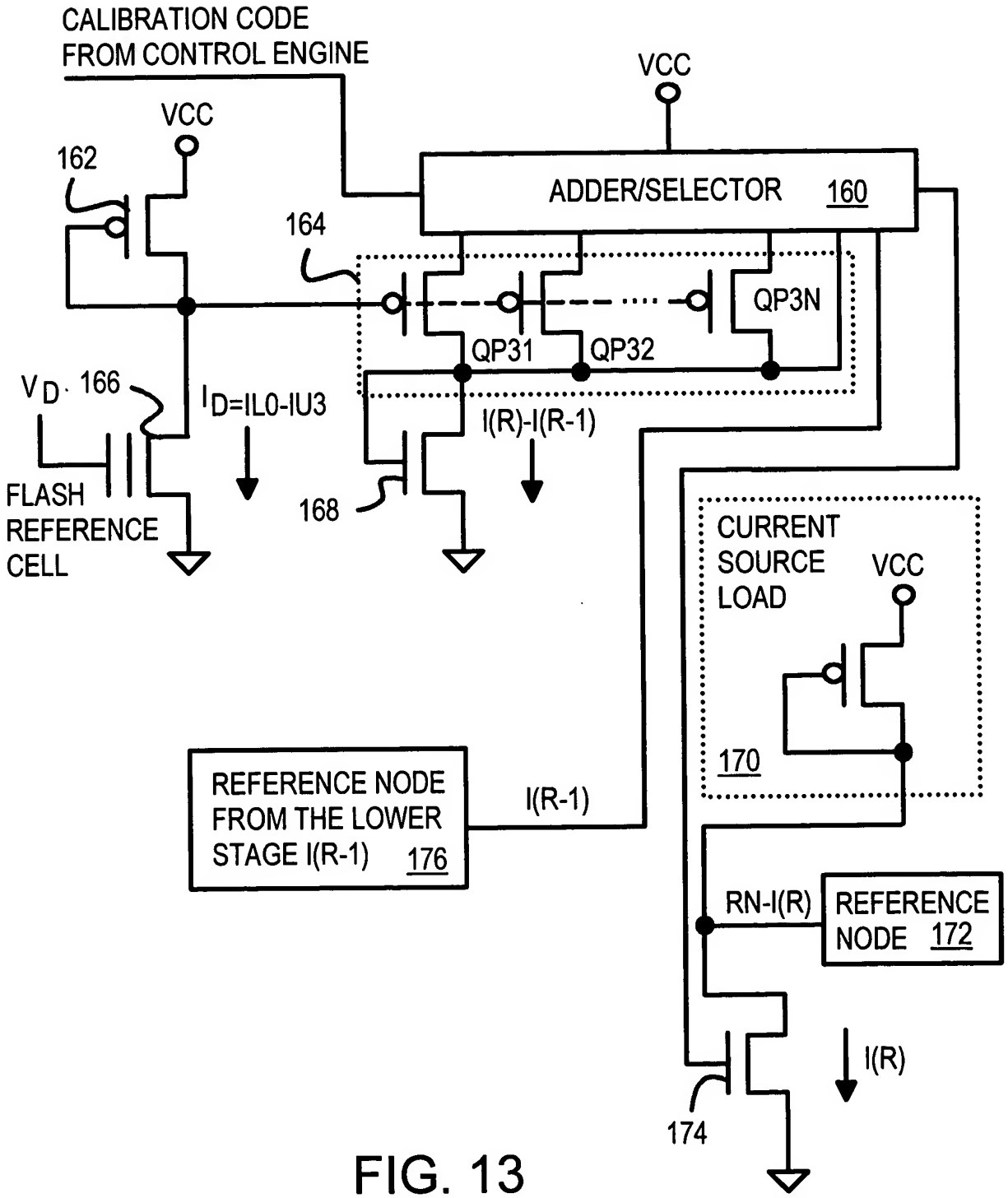

CALIBRATION CODE
FROM CONTROL ENGINE
VCC
VCC
162
ADDER/SELECTOR 160
164
QP3N
QP31
QP32
VD 166
ID=IL0-IU3
I(R)-I(R-1)
FLASH
REFERENCE
CELL
168
CURRENT
SOURCE
LOAD
VCC
170
REFERENCE NODE
FROM THE LOWER
STAGE I(R-1) 176
I(R-1)
RN-I(R)
REFERENCE
NODE 172
I(R)
174

FIG. 13

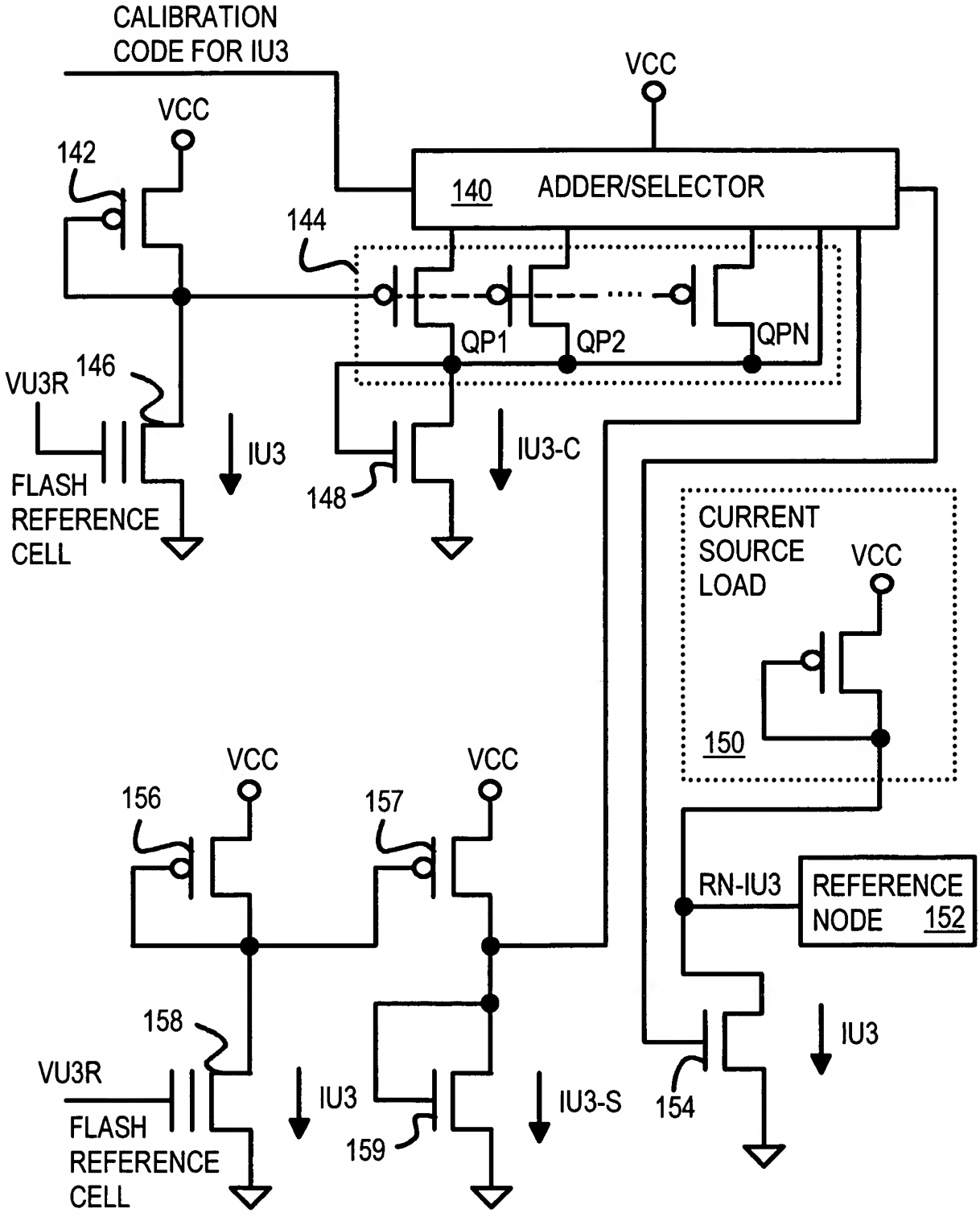

CALIBRATION
CODE FOR IU3
VCC
VCC
142
140
ADDER/SELECTOR
144
QP1
QP2
QPN
VU3R
146
IU3
IU3-C
FLASH
REFERENCE
CELL
148
CURRENT
SOURCE
LOAD
VCC
150
VCC
VCC
156
157
RN-IU3
REFERENCE
NODE
152
158
VU3R
IU3
IU3-S
IU3
154
159
FLASH
REFERENCE
CELL

FIG. 14